SEMICONDUCTOR DEVICE WITH A CHARGE CARRIER COMPENSATION STRUCTURE AND PROCESS

BACKGROUND

[0001] The application relates to a semiconductor device with a charge carrier compensation structure in a semiconductor body and a process for the production of same.

[0002] Semiconductor devices are used as power transistors and due to the charge carrier compensation structure achieve a R_{on} with significantly smaller chip areas than traditional power transistors. As a result their gate capacitances are considerably smaller, permitting them to be switched more quickly. However, they are at the same time more susceptible to vibrations and produce high voltage spikes due to their fast switching flanks. In such arrangements there is a fast drop in both gate-drain capacitance C_{GD}, also referred to as reverse transfer capacitance, and source-drain capacitance C_{SD} as supply voltage V_{DS} increases for certain applications. Extremely small capacitance values which exacerbate the disadvantages outlined above are reached even at moderate voltages V_{DS}.

[0003] For these and other reasons, there is a need for the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The accompanying drawings are included to provide a further understanding of the present invention and are incorporated in and constitute a part of this specification. The drawings illustrate the embodiments of the present invention and together with the description serve to explain the principles of the invention. Other embodiments of the present invention and many of the intended advantages of the present invention will be readily appreciated as they become better understood by reference to the following detailed description. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

[0005] FIG. **1** illustrates a schematic cross-section through a semiconductor device as disclosed in one embodiment;

[0006] FIG. **2** illustrates a schematic cross-section through a semiconductor device as disclosed in a further embodiment;

[0007] FIG. **3** illustrates a schematic cross-section through an alternative embodiment of the semiconductor device illustrated in FIG. **2**;

[0008] FIG. **4** illustrates a schematic cross-section through a semiconductor device as disclosed in a further embodiment;

[0009] FIG. **5** illustrates a schematic cross-section through a semiconductor device as disclosed in a further embodiment.

DETAILED DESCRIPTION

[0010] In the following Detailed Description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the Figure(s) being described. Because components of embodiments of the present invention can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

[0011] In one embodiment, a semiconductor device with a central cell field and a near-surface gate- and source structure is provided. The cell field is surrounded by an edge region with at least one bond contact area which is electrically connected to a gate structure or a source structure. Positioned beneath at least one part of at least one of the bond contact areas is a laterally extending, capacitance-increasing field plate which is insulated from the semiconductor body and electrically connected to at least one of the near-surface bond contact areas.

[0012] FIG. **1** illustrates a schematic cross-section through part of a semiconductor device **1** as disclosed in one embodiment. This part includes, on the right-hand side of FIG. **1**, a last cell of a cell field **9** of the semiconductor device **1** and, towards the left-hand side of FIG. **1**, an edge region extending to the edge **29** of a semiconductor chip of the semiconductor device **1**. In the area of the cell field **9** the semiconductor device **1** has a charge carrier structure **5** in a semiconductor body **6**, the semiconductor body **6** possessing an upper side **7** and a lower side **8**. As illustrated in FIG. **1**, a capacitance-increasing field plate **15** is connected to a near-edge trench gate electrode **20** of the cell field **9** and to a gate bond contact area **13**.

[0013] Towards the upper side **7** of the semiconductor body **6**, the charge carrier compensation structure **5** turns into a near-surface gate structure **10** and a source structure **11**. The central cell field **9** is surrounded by an edge region **12** with at least one gate electrode area **13** which may also be designed as a gate bond contact area and which, in one embodiment, is electrically connected to the gate structure **10**. Positioned between the gate bond contact area and the upper side **7** of the semiconductor body **6** are three layers: an intermediate insulating layer **17** which in one embodiment is positioned beneath the gate bond contact area **13**; a laterally extending, capacitance-increasing field plate **15** which extends from the edge of the cell field **9** over the majority of the edge region and ends before a channel stopper electrode **33**; and a field dielectric layer **18** positioned between a field plate **15** and the upper side **7** of the semiconductor body **6**. The field dielectric layer **18** is thus positioned beneath the gate bond contact area **13**. The field plate **15** is electrically connected to the gate potential via at least one contact via **16** through the field plate insulating layer **17**. As illustrated in FIG. **1**, the capacitance-increasing field plate **15** is thus connected both to a near-edge trench gate electrode **20** of the cell field **9** and to the gate bond contact area **13**. Instead of the trench gate electrodes **20** illustrated in FIGS. **1** to **4** it is also possible to use planar gate electrodes.

[0014] With a field plate **15** of this type it is possible to expand the space charge zone laterally in the edge region and to reduce its penetration depth in the semiconductor body **6**. This is illustrated by the equipotential lines **25** and **31** illustrated here by way of example. Equipotential line **25** illustrates approximately the maximum extent of the space charge zone in the cell field **9**. When the maximum possible voltage is applied it extends over almost the entire drift zone **26** as far as the transition to the semiconductor substrate **32**. In the edge region **12** the aim is to achieve the greatest possible capacitative effect by bringing the equipotential line **25** as close as possible to the upper side **7** of the semiconductor body **6** or